

IN THE SPECIFICATION:

Please amend the paragraphs beginning on page 2, line 6, as follows:

Japanese Patent Laid-open Publication No. HEI-6-85062 proposes an optimum cell layout by using variable height of wiring regions for inter-cell wirings in the cells. Wiring regions are disposed above a semiconductor active region, above the semiconductor active region and isolation region and the like. This Publication also proposes a broad wiring region formed by connecting wiring regions above the p-type and n-type active regions and common wirings formed in the broad wiring region.

Japanese Patent Laid-open Publication No. ~~HEI-4-263059~~ 6-85064 proposes that circuit information is developed into wiring information, single transistor cell information, serial cell information on a serial connection of a plurality of transistors and parallel cell information on a parallel connection of a plurality of transistors, respectively for n- and p-channel transistors. In a central area of a semiconductor chip, columns of n-type active regions and columns of p-type active regions are alternately disposed and a wiring region is disposed between adjacent active regions. Peripheral circuits are disposed in chip peripheral areas. Transistors having different channel lengths are distinguished from each other, making the size (channel length) of the column variable.